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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,882	09/19/2003	Darrell Rinerson	UNTYP027	6771

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EXAMINER	
KRAIG, WILLIAM F	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 08/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/665,882	RINERSON ET AL.	
	Examiner	Art Unit	
	William Kraig	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,8-14 and 19-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-14 and 19-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 31 is objected to because of the following informalities: There is a grammatical error in the claim. The claim, as understood by the Examiner, states that the treatment (to which the at least one interface is subjected) is directed towards changing properties of the perovskite. The Examiner recommends that the 2nd and 3rd lines of the claim be rewritten as --the treatment, to which the at least one interface is subjected, is directed towards changing properties of the perovskite--.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 8-14 and 19-31 rejected under 35 U.S.C. 102(e) as being anticipated by Zhuang et al. (U.S. Patent # 6759249) of record.

Regarding claim 1, Fig. 1 of Zhuang et al. discloses a resistive memory device comprising:

a conductive bottom electrode 14 having a top surface (on which layer 16 is disposed);

a multi-resistive state element 16 having a top surface (on which layer 18 is disposed) and a bottom surface (under which layer 14 is disposed), the bottom surface of the multi-resistive state element arranged on top of and in direct physical contact with the top surface of the conductive bottom electrode (see Fig. 1), the multi-resistive state element 16 having a substantially crystalline layer that (Col. 7, Lines 39-42 (Claim 18)), while substantially maintaining its substantially crystalline structure, has a modifiable resistance (Claim 20);

a conductive top electrode 18 having a bottom surface (under which layer 16 is disposed) and arranged on top of and in direct physical contact with the top surface of the multi-resistive state element (see Fig. 1);

a top interface (interface between layers 16 and 18) created by the direct physical contact between the bottom surface of the top electrode 18 and the top surface of the multi-resistive state element 16 (see Fig. 1); and

a bottom interface (interface between layers 14 and 16) created by the direct physical contact between the top surface of the bottom electrode 14 and the bottom surface of the multi-resistive state element 16 (see Fig. 1), at least one of the top interface or the bottom interface includes at least one treatment (Col. 3, Lines 13-33) primarily directed towards changing properties of the at least one interface (Claim 18) (Col. 7, Lines 39-42); and

whereby the properties of the at least one interface are changed by the at least one treatment (Claim 18) (Col. 7, Lines 39-42).

The claim to the resistance of the resistive memory device being changed by applying a first voltage having a first polarity across the conductive electrodes and being reversibly changed by applying a second voltage having a second polarity across the conductive electrodes is a purely functional limitation. It is well known that similar structures will, by their nature, have similar characteristics and functions. Thus, as the device of Zhuang et al. meets the structural limitations of this claim, it should also exhibit similar functional characteristics.

Regarding claim 2, Zhuang et al. discloses the resistive memory device of claim 1, wherein:

the at least one treatment causes a change in crystal structure (modifies a solid surface) at the at least one interface (Col. 3, Lines 34-37).

The claim to the at least one treatment being an ion implant is a product by process limitation and is given no patentable weight so long as the final product of said claim is the same as or obvious over the prior art. *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). The particular process of causing the change in crystal structure is therefore irrelevant given that the final product is anticipated by Zhuang et al.

Regarding claim 3, Zhuang et al. discloses the resistive memory device of claim 1, wherein:

the at least one treatment is an exposure to an anneal (Col. 3, Lines 13-33).

Regarding claim 4, Zhuang et al. discloses the resistive memory device of claim 3, wherein:

the anneal is performed while the multi-resistive state element is formed (Col. 3, Lines 13-33).

Regarding claim 5, Zhuang et al. discloses the resistive memory device of claim 1, wherein:

the at least one treatment is an exposure to a gas (Col. 3, Lines 13-33).

Regarding claim 8, Zhuang et al. discloses the resistive memory device of claim 3, wherein:

the anneal is performed after the conductive bottom electrode is formed (Claim 18) (Col. 7, Lines 45-51).

Regarding claim 9, Zhuang et al. discloses the resistive memory device of claim 3, wherein:

the anneal is performed after the multi-resistive state element is formed (Claim 18) (Col. 7, Lines 45-51).

Regarding claim 10, Zhuang et al. discloses the resistive memory device of claim 3, wherein:

the anneal is performed after the conductive top electrode is formed (Claim 18) (Col. 7, Lines 45-51).

Regarding claim 11, Zhuang et al. discloses the resistive memory device of claim 5, wherein:

there is a chemical reaction in the multi-resistive state material (Col. 7, Lines 39-42).

The claim to the exposure to the gas causing said chemical reaction in the multi-resistive state material is a product by process limitation and is given no patentable weight so long as the final product of said claim is the same as or obvious over the prior art. *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). The particular process of causing the chemical reaction is therefore irrelevant given that the final product is anticipated by Zhuang et al.

Regarding claim 12, Zhuang et al. discloses the resistive memory device of claim 5, wherein:

the exposure to the gas is performed after the conductive bottom electrode is formed (Claim 18) (Col. 7, Lines 45-51).

Regarding claim 13, Zhuang et al. discloses the resistive memory device of claim 5, wherein:

the exposure to the gas is performed after the multi-resistive state element is formed (Claim 18) (Col. 7, Lines 45-51).

Regarding claim 14, Zhuang et al. discloses the resistive memory device of claim 5, wherein:

the exposure to the gas is performed after the conductive top electrode is formed (Claim 18) (Col. 7, Lines 45-51).

Regarding claims 19, 20 and 21, Zhuang et al. discloses the resistive memory device of claim 1.

The claims to the at least one treatment being caused by a chemical reaction between one of the conductive electrodes and the multi-resistive state element and to said chemical reaction being caused by an anneal process or exposure to a gas are product by process limitations and are given no patentable weight so long as the final product of said claims are the same as or obvious over the prior art. *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). The particular process of causing the treatment is therefore irrelevant given that the final product is anticipated by Zhuang et al.

Regarding claims 22 and 23, Zhuang et al. discloses the resistive memory device of claim 1.

The claims to the at least one treatment being caused by a plasma process/plasma etch are product by process limitations and are given no patentable

weight so long as the final product of said claims are the same as or obvious over the prior art. *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). The particular process of causing the treatment is therefore irrelevant given that the final product is anticipated by Zhuang et al.

Regarding claim 24, Zhuang et al. discloses the resistive memory device of claim 1, wherein:

both the bottom interface (interface between layers 14 and 16) and the top interface (interface between layers 16 and 18) are subject to a treatment, the treatments being different from each other (Col. 3, Lines 13-33).

Regarding claim 25, Zhuang et al. discloses the resistive memory device of claim 1, wherein:

the at least one treatment is caused by re-sputtering (Col. 3, Lines 13-33 and Col. 3, Lines 62-65).

Regarding claims 26 and 27, Zhuang et al. discloses the resistive memory device of claim 1.

The claims to the at least one treatment being caused by a bombardment of inert ions or a laser treatment are product by process limitations and are given no patentable weight so long as the final product of said claims are the same as or obvious over the prior art. *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). The

particular process of causing the treatment is therefore irrelevant given that the final product is anticipated by Zhuang et al.

Regarding claim 28, Zhuang et al. discloses a resistive memory device comprising:

a conductive bottom electrode 14 having a top surface (on which layer 16 is disposed);

a multi-resistive state element 16 having a top surface (on which layer 18 is disposed) and a bottom surface (under which layer 14 is disposed), the bottom surface of the multi-resistive state element arranged on top of and in direct physical contact with the top surface of the conductive bottom electrode (see Fig. 1), the multi-resistive state element 16 having at least one layer that is fabricated to be substantially crystalline (Col. 7, Lines 39-42 (Claim 18)) and have a programmable resistance (Claim 20);

a conductive top electrode 18 having a bottom surface (under which layer 16 is disposed) and arranged on top of and in direct physical contact with the top surface of the multi-resistive state element (see Fig. 1);

a top interface (interface between layers 16 and 18) created by the direct physical contact between the bottom surface of the top electrode 18 and the top surface of the multi-resistive state element 16 (see Fig. 1); and

a bottom interface (interface between layers 14 and 16) created by the direct physical contact between the top surface of the bottom electrode 14 and

the bottom surface of the multi-resistive state element 16 (see Fig. 1), at least one of the top interface or the bottom interface includes a treatment (Col. 3, Lines 13-33) primarily directed towards changing properties of the at least one interface (Claim 18) (Col. 7, Lines 39-42); and

whereby the properties of the at least one interface are changed by the at least one treatment (Claim 18) (Col. 7, Lines 39-42).

The claim to the resistance of the resistive memory device being programmed by applying a first voltage having a first polarity across the conductive electrodes and being reversibly programmed by applying a second voltage having a second polarity across the conductive electrodes is a purely functional limitation. It is well known that similar structures will, by their nature, have similar characteristics and functions. Thus, as the device of Zhuang et al. meets the structural limitations of this claim, it should also exhibit similar functional characteristics.

Regarding claim 29, Zhuang et al. discloses the resistive memory device of claim 28, wherein:

the at least one layer 16 that is fabricated to be substantially crystalline (Col. 7, Lines 39-42 (Claim 18)) is fabricated to be polycrystalline (Col. 2, Lines 53-54).

Regarding claim 30, Zhuang et al. discloses the resistive memory device of claim 28, wherein:

the at least one layer that is fabricated to be substantially crystalline 16 is fabricated to be a perovskite (PCMO) (Col. 1, Lines 15-20) (Col. 3, Lines 13-33).

Regarding claim 31, Zhuang et al. discloses the resistive memory device of claim 30, wherein:

the treatment, to which the at least one interface is subjected, is directed towards changing properties of the perovskite (Col. 7, Lines 39-42).

Response to Arguments

Applicant's arguments filed 5/4/2006 have been fully considered but they are not persuasive.

Applicant first argues that the interface between 16b and 18 (or between 14 and 16a) does not inherently or explicitly include an interface created by a direct physical contact between a top/bottom surface of the PCMO layer and a bottom/top surface of the top/bottom electrode. The Examiner argues that Zhuang et al. does indeed disclose this interface created by direct physical contact. Fig.1 of Zhuang et al. discloses the top electrode 18 being formed directly on top of the PCMO layer 16 and the PCMO layer 16 being formed directly on top of the bottom electrode 14. Furthermore, an interface is defined simply as a surface forming a common boundary between adjacent regions, bodies, substances, or phases. These surfaces can be seen in Fig. 1 as the point where layers 18 and 16 contact one another and the point where layers 14 and 16 contact each other.

Applicant further argues that Zhuang et al. does not disclose said interfaces including at least one treatment, or said interfaces being changed by the treatment. Examiner argues that, as the interface is simply the surface forming a common boundary between adjacent regions, bodies, substances, or phases, the interface includes the surface of each layer (14, 16 and 18). Examiner further argues that, because Zhuang et al. teaches (Col. 3, Lines 13-33) that layers 16 are treated in various ways and are changed by this treatment (Col. 3, Lines 34-37) (Col. 7, Lines 39-42), that Zhuang et al. does indeed disclose the interface including the treatment and being changed by the treatment.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Kraig whose telephone number is 571-272-8660. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

WFK
07/19/2006

EUGENE LEE
PRIMARY EXAMINER